REMARKS

Claims 14-17 and 53-80 are pending in the present application.

Claims 14-16, 53-56, and 59-67 stand rejected under 35 USC 103(a) for obviousness over U.S. Patent No. 5,475,317 to Smith et al. Claims 69-72, 74-8, and 80 stand rejected under 35 USC 112, first paragraph.

Applicant notes that no rejections are presented with respect to claims 17, 57-58, 68, 73 and 79. Accordingly, Applicants request examination of such claims in a ***non-final action*** if such claims are not found to be allowable. In particular, Applicant respectfully asserts that the Office Action clearly fails the regulatory mandate of 37 CFR 1.104(b) that "the examiner's action will be complete as to all matters." the Office Action clearly fails the regulatory mandate of 37 CFR 1.104(c)(2) requiring that "the pertinence of each reference, if not apparent, must be clearly explained." Applicants request a new ***non-final office action*** completely addressing all matters currently of record if the above-identified claims are not found to be allowable.

The 112, first paragraph rejection is in error. The rejected claims are supported by the originally filed application and the specification includes numerous teachings of processing workpieces and wafers. It is known and inherent that such processing occurs prior to die singulation.

For example, page two of the application refers to chemically amplified resists which are utilized in deep ultraviolet (DUV) lithography and small micron geometries. Also on page 2, lines 8-12, it is stated that workpiece temperature and workpiece temperature uniformity are parameters which are closely monitored during wafer and workpiece

fabrication. As set forth on page 4 of the specification, exemplary sensors include resistance temperature devices configured to provide process signals containing process information regarding the electronic device workpiece processing apparatus. As set forth on page 2, lines 22-24, temperature sensors across the surface of a wafer are utilized to provide temperature mapping of a workpiece during processing. On page 7, lines 13-19, it is stated that workpieces typically undergo processing from which subsequent devices are formed. Exemplary workpieces include semiconductor wafers, glass or quartz substrates for flat panel or field emission display devices. It is also stated on page 7 that typical production workpieces are processed and subsequently utilized to form products used in a variety of electronic devices. On page 9, lines 4-8, it is stated that process signals provided by sensors 23 and corresponding to processing conditions of workpiece 21 are received within data gathering device 14. Alterations to processing conditions of apparatus 10 can be changed responsive to the reception of the process signals within device 14. On page 16, lines 7-9, it is stated that chuck 40 is isolated to a greater extent from a processing environment utilized to fabricate or process electronic device workpieces. On page 17, lines 3-6, it is stated that one configuration of apparatus 10 of Fig. 6 enables processing of production workpieces while monitoring processing conditions using calibration workpiece 20. Referring to page 19, lines 12-19, it is stated that layer 28 operates to protect surface 21, sensor 23, and electrical connection 27 from the processing environment including gases, chemicals, plasmas, etc. utilized during processing of electronic device workpieces.

Accordingly, the originally filed specification is replete with teachings of processing a workpiece, such as a wafer, within a workpiece processing apparatus (see reference 10 of the originally-filed specification). The disclosure of the originally filed specification provides support for the claimed subject matter especially with reference to the disclosed exemplary embodiments of electronic device workpiece processing apparatus 10 and processing of workpieces 20 as described in the originally filed specification.

In addition, Applicant refers the Examiner to U.S. Patent Application Serial No. 09/032,184 incorporated into the subject application by reference as set forth on page 3, lines 9-15 of the originally filed specification. Serial No. 09/032,184 includes additional teachings providing support of the pending claims.

For example, Applicant refers the Examiner to the following teachings on page 17, line 11 - page 18, line 17 of the '184 application providing:

> In some embodiments, the described electronic device workpiece is configured and utilized as a calibration wafer. Such calibration wafers are typically placed within a workpiece processing chamber and the chamber can be brought up to subject processing conditions at typical elevated temperatures. Through the use of an electronic device workpiece configured as a calibration wafer, the temperature at various positions upon electronic device workpieces to be processed can be determined. Thereafter, data provided by temperature sensing devices located upon the electronic device workpiece can be utilized to provide temperature control and modify some aspect of the processing chamber.

The processing chamber is preferably modified to provide a uniform temperature distribution across the entire surface of the electronic device workpiece being processed. In other processes, the processing chamber is modified to provide varied temperatures across a surface of the workpiece.

The modifications can be made with the calibration workpiece in place within the processing chamber. The effect of such modifications can be verified by the temperature sensing devices and associated temperature monitoring equipment coupled with the devices. Thereafter, the calibration workpiece is removed and the equipment having been desirably calibrated can be utilized to process other electronic device workpieces in mass.

In another embodiment, temperature sensing devices are provided upon an electronic device workpiece which will actually be processed and subsequently utilized to fabricate integrated circuitry or other components. The temperature sensing devices can be fabricated upon the electronic device workpiece during the fabrication of the electronic device workpiece. In another embodiment, preexisting or prefabricated temperature sensing devices are positioned and adhered upon the electronic device workpiece.

Additional teachings providing support in the '184 application may be found at page 1, line 10 - page 3, line 9; page 5, lines 1-4; page 6, lines 11-19; page 14, line 14 - page 15, line 4; page 11, lines 13-22; and page 15, line 21 - page 16, line 15. Further regarding the rejection based on §112, first paragraph, the Examiner is respectfully reminded that MPEP §2163.02 (8th Edition) states the test for sufficiency of support in a application is

whether the disclosure relied upon "reasonably conveys to the artisan that the inventor had possession at that time of the later claimed subject matter." MPEP §2163.02 (8th Edition) *citing Ralston Purina Co. v Far-Mar-Co., Inc.*, 772 F.2d 1570, 1575, 227 USPQ 177, 179 (Fed. Cir. 1985). Notably, the subject matter of the claim need not be described literally (i.e., **using the same terms** or *in haec verba*) in order for the disclosure to satisfy the description requirement. MPEP §2163.02 (8th Edition).

MPEP §2163 I. (8th Edition) states it is now well accepted that a satisfactory description may be in the claims or any other portion of the originally-filed specification and an applicant shows possession of the claimed invention by describing the claimed invention with all of its limitations using such descriptive means as words, structures, figures, diagrams, and formulas that fully set forth the claimed invention (citations omitted).

The claims are supported by the originally filed application and the specification includes numerous teachings at least as identified above. MPEP Section 2163.07(a) (8th ed.) states that *by disclosing in a patent application a device that inherently performs a function or has a property, operates according to a theory or has an advantage, a patent application necessarily discloses that function, theory or advantage, even though it says nothing explicit concerning it. The application may later be amended to recite the function, theory or advantage without introducing prohibited new matter.* *In re Reynolds*, 443 F.2d 384, 170 USPQ 94 (CCPA 1971); *In re Smythe*, 480 F.2d 1376, 178 USPQ 279 (CCPA 1973).

It is clear applicants have disclosed processing a wafer or other workpieces (e.g., reference 10 of the originally-filed specification) that inherently performs the function of

processing workpieces or wafers. In accordance with the MPEP, Applicant's claiming of exemplary functions of apparatus 10 is not new matter.

Applicants note MPEP 2163 II. A. (8th ed.), states *the Examiner has the initial burden, after a thorough reading and evaluation of the content of the application, of* ***presenting evidence or reasons*** *why a person skilled in the art would not recognize that the written description of the invention provides support for the amendment.* Further, it is stated that if applicant points out where a claim is supported, the Examiner has the initial burden of presenting evidence or reasoning to explain why persons skilled in the art would not recognize in the disclosure a description of the invention defined in the claims.

Further, MPEP §2163.111.A (8th ed.) provides:

> In rejecting a claim, the examiner must set forth express findings of fact regarding the above analysis which support the lack of written description conclusion. These findings should:
>
> (A) Identify the claim limitation at issue; and
>
> (B) Establish a *prima facie* case by providing reasons why a person skilled in the art at the time the application was filed would not have recognized that the inventor was in possession of the invention as claimed in view of the disclosure of the application as filed. A general allegation of "unpredictability in the art" is not a sufficient reason to support a rejection for lack of adequate written description.

The Office Action merely states "it appears that the specification does not have support for the limitations" with no evidence or reasoning. Such fails the clear mandate of

the MPEP. Applicant respectfully request clarification of the 112, first paragraph, rejections in a ***non-final action*** if such rejection is maintained in the next Action so Applicant may appropriately respond.

Referring to the obviousness rejection of claim 14, Applicant disagrees with the statement that it would have been obvious for one of ordinary skill in the art to use the device of Smith to test the wafer since both of the devices "have the same characteristics" as set forth on page 2 of the Office Action. Once again, Applicant refers the Examiner to the Van Zandt reference illustrating the clear differences between a wafer and a singulated die. Further, the explicit teachings of Smith discuss the differences between wafer and singulated die apparatus and the inapplicability of one device to the other. More specifically, Applicant refers the Examiner to the unambiguous teachings of the Smith reference clearly distinguishing die testing and wafer testing at col. 1, lines 45-56. Further, col. 2, lines 10-16 state that probe cards designed to contact wafers are designed to contact entire wafers and *are not intended for testing bare singulated die and the cards cannot be used to test bare die*. Clearly, as set forth in the explicit Smith teachings, it is observed in the art that wafers and singulated die do not have the same characteristics as alleged in the Office Action. Further, the Office Action recites absolutely no evidence in support of the bald, cursory statement. The 103 rejection is based upon statements contrary to the explicit reference teachings and must be withdrawn.

As set forth on page 3 of the Office Action, Smith discloses a *singulated bare die tester*. As set forth in the abstract, Smith discloses a reusable test socket for testing *singulated bare die*. Smith is only related to testing of singulated bare dies.

The body of claim 14 positively defines an ***electronic devic wafer proc ssing intermediat member*** *adapted to receive an* ***electronic d vice wafer***. Applicant has electronically searched the embodiments of the detailed description of Smith and have failed to uncover any wafer teachings. The reference teachings of Smith concerning testing of a singulated bare die in no fair interpretation disclose or suggest the positively recited wafer limitations of claim 14. Accordingly, Smith fails to teach or suggest limitations of claim 14. Claim 14 is patentable over the prior art for at least this reason.

Claim 14 stands rejected for obviousness over Smith. Referring to MPEP §2143.01 (8th ed.), there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify or combine reference teachings. The mere fact that references *can* be combined or modified does not render the resultant combination obvious *unless the prior art also suggests the desirability of the combination.* MPEP §2143.01 *citing In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Obviousness cannot be established by a combination of references unless there is some motivation in the art to support the combination. *See ACH Hospital Systems, Inc. v. Montifiore Hospital*, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). The motivation for forming the combination must be something other than hindsight reconstruction based on using Applicant's invention as a road map for such a combination. *See, e.g., Interconnect Planning Corp. v. Feil*, 227 USPQ 543, 551 (Fed. Cir. 1985); *In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990).

The Office Action states that the 103 rejection is proper because wafers and singulated die allegedly have "the same characteristics." Initially, such statement is entirely

contrary to the explicit teachings of Smith and fails to provide proper motivation. Smith is entirely directed towards problems concerned with alignment of singulated die (col. 3, lines 40-63) and with testing die after separation from the wafer when defects may be introduced (col. 1, lines 52-56). Smith is replete with teachings evidencing die and wafers do not have the same characteristics as alleged.

Second, assuming *arguendo*, wafers and singulated die have the same characteristics, such is improper motivation to combine reference teachings and only motivation can only result from improper utilization of Applicant's disclosure.

Further, the motivation to combine because the "devices have the same characteristics" is insufficient to support the 103 rejection. The Federal Circuit discussed proper motivation *In re Lee*, 61 USPQ 2d 1430 (Fed. Cir. 2002). The motivation identified in the Office Action is akin to the conclusory statements set forth in *In re Lee* which were found to fail to provide the requisite motivation to support an obviousness rejection. The Court in *In re Lee* stated the factual inquiry whether to combine references must be through and searching. It must be based on objective evidence of record. The Court in *In re Fritch*, 23 USPQ 2d 1780, 1783 (Fed. Cir. 1992) stated motivation is provided only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. The *Lee* Court stated that the Examiner's conclusory statements in the *Lee* case do not adequately address the issue of motivation to combine. The Court additionally stated that the factual question of motivation is material to patentability and can not be resolved on subjective belief and unknown authority. The Court also stated that

deficiencies of cited references cannot be remedied by general conclusions about what is basic knowledge or common sense. The Court further stated that the determination of patentability must be based on evidence.

In the instant case, the record is entirely devoid of any evidence to support motivation to combine the teachings apart from the bald conclusory statements of the Examiner which are insufficient for proper motivation as set forth by the Federal Circuit. The Office cannot rely on conclusory statements when dealing with particular combinations of prior art and specific claims but must set forth rationale on which it relied. Statements set forth in the present Office Action are akin to the alleged motivation discussed *In re Lee* and accordingly are insufficient to combine the reference teachings. The 103 rejection of claim 14 is improper without the proper motivation and Applicants respectfully request allowance of claim 14 in the next action.

The claims which depend from independent claim 14 are in condition for allowance for the reasons discussed above with respect to the independent claim as well as for their own respective features which are neither shown nor suggested by the cited art.

Claim 16 stands rejected because, in the Examiner's opinion, it would have been "well known" to consider that a selection of a "pogo pin" as an obvious design choice. Applicant hereby traverses the assertion of judicial notice and requests the submission of prior art or an affidavit from the Examiner in accordance with MPEP 2144.03.

The Examiner is reminded that the facts constituting the state of the art are normally subject to the possibility of rationale disagreement among reasonable men and are not amenable to the taking of judicial notice. See *In re Eynde*, 480F.2d 1364, 1370, 178

USPQ 470, 474 (CCPA 1973). The Examiner is also reminded that claims are analyzed in the context of the combination of the various separately stated limitations, and not with respect to the limitations individually. Pursuant to MPEP §2144.03 (8th ed.), Applicant hereby demands evidence with respect to what the Examiner apparently relies upon as being "well-known." Claim 16 is allowable without additional prior art or an affidavit in support of the 103 rejection in view of Applicant's traversal.

Claim 54 recites a first surface configured to support substantially an entirety of an ***electronic device wafer*** and a second electrical coupling adjacent to the second surface and *configured to electrically connect with an electrical coupling of a chuck of* ***the wafer processing apparatus.*** Claim 54 is allowable over the prior art.

Initially, the reference teachings of Smith concerning testing of a singulated bare die in no fair interpretation disclose or suggest the positively recited wafer limitations of claim 54. Accordingly, Smith fails to teach or suggest limitations of claim 54 and the claim is patentable over the Smith reference for at least this reason.

In addition, the die testing apparatus of Smith fails to disclose or suggest the wafer processing apparatus defined in claim 54. The wafer processing apparatus is clearly positively-recited in the body of claim 54 and is not taught nor suggested by Smith. The rejection of claim 54 is improper for this additional reason.

There is no motivation to modify the Smith reference teachings and claim 54 is allowable for this additional reason.

The claims which depend from independent claim 54 are in condition for allowance for the reasons discussed above with respect to the independent claim as well as for their own respective features which are neither shown nor suggested by the cited art.

Claim 61 recites an intermediate member comprising an electrical interconnect configured to electrically connect an electrical coupling of an ***electronic device wafer*** with *an electrical coupling of a chuck of the* ***wafer processing apparatus***, and wherein the electrical interconnect is configured to communicate electrical signals intermediate the electrical coupling of the wafer and the electrical coupling of the chuck. Claim 61 is allowable over the prior art.

The reference teachings of Smith concerning testing of a singulated bare die in no fair interpretation disclose or suggest the positively recited wafer limitations of claim 61. Accordingly, Smith fails to teach or suggest limitations of claim 61 and the claim is patentable over the Smith reference for at least this reason.

In addition, the die testing apparatus of Smith fails to disclose or suggest the wafer processing apparatus defined in claim 61. The wafer processing apparatus is clearly positively-recited in the body of claim 61 and is not taught nor suggested by Smith. The rejection of claim 61 is improper for this additional reason.

There is no motivation to modify the Smith reference teachings and claim 61 is allowable for this additional reason.

The claims which depend from independent claim 61 are in condition for allowance for the reasons discussed above with respect to the independent claim as well as for their own respective features which are neither shown nor suggested by the cited art.

For example, referring to claim 65, it is stated on page 3 of the Office Action, that it would have been "well-known" that the board of Smith is the equivalent to the data gathering device. There is no "data gathering device" claimed in claim 65 and the rejection therefor is accordingly nonsensical. Applicant requests a proper rejection of claim 65 in a ***non-final action*** in accordance with 37 CFR 1.104 if such claim is not found to be allowable in the next Action.

Numerous claimed limitations are not shown nor suggested by the prior art. In the event that a rejection of the claims is maintained with respect to the prior art, or a new rejection made, Applicants respectfully request identification *in a* ***non-final action*** of elements which allegedly correspond to limitations of the claims in accordance with 37 C.F.R §1.104(c)(2). In particular, 37 C.F.R §1.104(c)(2) provides that *the pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified.* Further, 37 C.F.R. §1.104(c)(2) states that the Examiner must cite the best references at their command. When a reference is complex or shows or describes inventions other than that claimed by Applicants, the particular teachings relied upon must be designated as nearly as practicable. The pertinence of each reference if not apparent must be clearly explained for each rejected claim specified. Applicants respectfully request clarification of the rejections with respect to specific references and specific references teachings therein pursuant to 37 C.F.R. §1.104(c)(2) in a ***non-final*** *action* if any claims are not found to be allowable.

Support for the amendments may be found with respect to the teachings of reference 10 of the originally-filed specification and associated text and Figures including at least the teachings specifically identified above.

Applicant notes that reference AE has not been initialed on the form PTO-1449 filed April 2, 2001. Applicant respectfully requests initialization of the references on a form PTO-1449 (copy enclosed for the Examiner's convenience) and return of the initialed form to Applicant indicating full consideration of the references by the Examiner in compliance with obligations set forth in MPEP §609 (8th ed.). Applicant respectfully requests a telephone call if the references are not considered so Applicant may properly respond to have the references considered during the prosecution of the present application.

Applicant respectfully requests allowance of all pending claims.

The Examiner is requested to phone the undersigned if the Examiner believes such would facilitate prosecution of the present application. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: 3/13/03

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